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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/761,494	01/16/2001	Micah C. Knapp	5160-02	5895

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EXAMINER	
PAN, DANIEL H	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 06/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/761,494	KNAPP ET AL.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 January 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *12-14* is/are allowed.

6)☐ Claim(s) *1,2,15,16,26 and 27* is/are rejected.

7)☒ Claim(s) *3-11,17-25 and 28-32* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *01/16/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-32 are presented for examination.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1,2, 15, 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Keller et al. (6,622,237) in view of Fetterman et al. (5,553,256).

As to claims 1, 15, Keller disclosed a superscalar system including at least :

a) execution units for executing in-flight instructions (e.g. see fig.1 [40] AB);

b) plurality of physical registers (e.g. see col.6, lines 41-58);

c) rename unit [34] (see col.6, lines 60-67, col.7, lines 1-12) for renaming architectural register to physical registers :

c) scheduling unit (see fig.3 [36] including a dependency matrix for storing dependent data (see dependent data stored in buffer 66 in col.11, lines 9-44), and a wait buffer for storing physical address [PA] (e.g. see the physical address stored in col.11, lines 58-67, col.12, lines 1-22)) when the dependency was removed (see the satisfied condition of ht dependency determined by the scheduler 36 in col.11, lines 27-44);

d) a content addressable memory circuit (see fig.3 [60][62], see fig.4 for more detailed structure, see the Table 82 was a CAM memory with other functional elements in the figure), the CAM circuit generating dependency data (see the dependency output and

dependency valid signal in col.10. lines 35-55, col.14, lines 23-58, col.15, lines 24-39), and for generating physical address (see the physical address was assigned according to the R#s in col.7, lines 2-8).

3. Keller did not specifically show his CAM had a comparator mapped to an array section as claimed. However, Fetterman disclosed a system including a CAM having comparator [240 OR] mapped to an array section (e.g. see comparator 900 in the CAM, see the CAM portion in fig.9, see also detailed AM array in fig.2). It would have been obvious to one of ordinary skill in the art o use Fetterman for including a CAM having a comparator mapped to an array section as claimed because the use of Fetterman could provide Keller the ability to accept result of the source registers based on the valid bit of the specific matching portions of CAM memory from the respective concurrently executed instructions, and thereby increasing the processing bandwidth of the CAM array , and it could be readily achieved by reconfiguring the mapped comparator of Fetterman into Keeler with the modified control read/write ports so that the mapped comparator could be recognized by Keller in order to achieve greater processing bandwidth, and in doing so, provided motivation.

4. As to claims 2, 16, Fetterman also included a logical gate ,NOR, at the outputs of the Cam cells (e.g. see col.15, lines 34-49). The claim recites OR logic while Fetterman disclosed at NOR at the output cells. However, since no advantages of using OR instead of NOR can be found either in the specification or in the claim, it is

assumed any logic combination of the CAM cells outputs would be based on the architecture options or preferences , and not affecting the main scope of the invention. Applicant is welcome to provide feedback in the next response.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 26,27 are rejected under 35 U.S.C. 102(e) as being anticipated by Keller et al (6,622,237).

6. As to claim 26, Keller disclosed at least :

a) fetching instructions (see the fetching of instructions in col.4, lines 65-67);

b) renaming architectural registers associated with instructions to physical registers (e.g. see the renaming file 34 in col.6, lines 65-67, col.7, lines 1-12);

c) transmitting first output signal from a CAM structure (see fig.4) for generating dependency data (see the output of dependency data in fig.4);

d) transmitting a second output signal from the CAM structure (see fig.4) for generating physical address necessary to execute the instructions (e.g. see col. (see output [R#] to dependency unit 62, see col.7, lines 1-8 for the physical address of the registers based on the R#s) when the dependency data indicates the dependency was

removed (see the dependency condition satisfied in col.11, lines 8-44), see the dependency data storing buffer 66);

e) storing dependency data in a matrix (see the buffer 66 in fig.3);

storing the physical address in a wait buffer (e.g. see the PA stored in PA Buffer 70 in fig.3);

f) scheduling execution based on the dependency data and physical address (see the operation the schedulable 36 in col.11, lines 38-61).

7. As to the language "in-flight instruction, the in-flight instructions are read as the instruction waiting before execution in view of the reading from the applicant's specification (e.g. page 2, lines 18-24). Therefore, any instructions before the executions are in-flight instructions.

8. As to claim 27, Fetterman also included a logical gate ,NOR, at the outputs of the Cam cells (e.g. see col.15, lines 34-49). The claim recites OR logic while Fetterman disclosed a NOR at the output cells. However, since no advantages of using OR instead of NOR can be found either in the specification or in the claim, it is assumed any logic combination of the CAM cells outputs would be based on the architecture options or preferences , and not affecting the main scope of the invention. Applicant is welcome to provide feedback in the next response.

9. Claims 3 , 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of

the base claim and any intervening claims. None of prior art of record further teaches the maximum number of registers source and the maximum number of the register destination fields, and each CAM dedicated to a single CAM.

10. Claims 4-11, 18-25 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the register dependency checker in the comparator section for comparing the RS field of the fetched instruction to RD filed of in-flight instruction and the hit signal indicating the architectural address of the RD between the RS field and the RD field, and the hit bit additionally being transferred tot eh array section of CAM.

11. Claims 12-14 are allowable over the art of record for reciting the combined features of the instruction scheduling unit, the first number of the content addressable memory having the comparator mapped to the array section, the single RS field , the transmitted OR signals together at the Oring unit and the output signals for each CAM combined to generate the physical address stored in the IWB.

12. Claims 28-32 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further

teaches the maximum number of register source fields, the comparison of the RS field to the RD fields, the hit signal, and the transmission of the hit signal to the array section.

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Moreno et al. (5,918,005) is cited for the basic teaching of the mapping of specific memory address space and region in an out-of-order instruction processing system (e.g. see col.12, lines 47-67).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

21 Century Strategic Plan

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PRIMARY EXAMINER
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